WHAT IS CLAIMED IS:

1. A memory circuit for storing and providing streams of data, said memory circuit accommodating both serial access and random access, and said memory circuit comprising:

a random access memory array having an address input and a data port;

a data buffer having a data port coupled to said memory array data port, said data buffer synchronizing operation of said memory array to the streams of data;

an address sequencer having a data input and having an output coupled to said memory array address input, said address sequencer generating a sequence of memory addresses to be successively applied to said memory array; and

an address buffer register having an output coupled to said address sequencer data input, said address buffer register supplying a random access address that initializes the sequence of memory addresses generated by said address sequencer.

2. A memory circuit as claimed in Claim 1 wherein said address buffer register comprises a serially loaded shift register.

3. A memory circuit as claimed in Claim 1 additionally comprising a terminal coupled to said address sequencer and adapted to receive a signal which causes data contained in said address buffer register to transfer to said address sequencer.

4. A memory circuit as claimed in Claim 1 wherein said memory array, data buffer, address sequencer, and address buffer register are included within a single integrated circuit.

5. A memory circuit as claimed in Claim 1 wherein said address sequencer comprises a binary counter having a data input coupled to the output of said address buffer register and an output coupled to the address input of said memory array.

6. A memory circuit as claimed in Claim 1 wherein said address sequencer comprises:

a first register having a data input coupled to a node which serves as said address sequencer data input and an output which serves as said address sequencer output;

a second register having an output, said second register being for storing an increment step value; and

an adder having a first input coupled said first register output, a second input coupled to said second register output, and an output coupled to said first register data input.

7. A memory circuit as claimed in Claim 1 wherein said data buffer synchronizes operation of said memory array to the data stream being stored into said memory array, said address sequencer generates memory addresses at which the stored data stream is written into said memory array, and said memory circuit additionally comprises:

a second data buffer having a data port coupled to said memory array data port, said second data buffer

being for synchronizing operating of said memory array to the data stream provided by said memory circuit;

a second address sequencer having an output coupled to said memory array address input and a data input, said second address sequencer generating a sequence of memory addresses to be applied to said memory array for reading the provided data stream from said memory array; and

a second address buffer register having an output coupled to said second address generator data input, said second address buffer register supplying a random access address that initializes the sequence of memory addresses generated by said second address sequencer.

8. A memory circuit as claimed in Claim 1 additionally comprising:

an address offset register having an output, said address offset register being for storing address offset data; and

an adder having a first input coupled to said address buffer register output, a second input coupled to said address offset register output, and an output coupled to a data input of said address buffer register, said adder providing a random access address representing a sum of a past random access address and said address offset data.

9. A memory circuit as claimed in Claim 1 additionally comprising an alternate address buffer register having an output coupled to said address sequencer data input, said alternate address buffer register supplying an alternate random access address that

initializes an alternate sequence of memory addresses generated by said address sequencer.

10. An integrated memory circuit for storing and providing streams of data, said integrated memory circuit accommodating serial access and limited random access, and said integrated memory circuit comprising:

a random access memory array having an address input, a data input port, and a data output port;

a first data buffer having a data port coupled to said memory array data input port, said first data buffer synchronizing operation of said memory array to the stored stream of data;

a second data buffer having a data port coupled to said memory array data output port, said second data buffer synchronizing operation of said memory array to the provided stream of data; and

first and second address generators wherein said first address generator generates addresses used for writing the stored data stream into said memory array, said second address generator generates addresses used for reading the provided data stream from said memory array, and each of said first and second address generators comprises:

a binary counter having an output coupled to said memory array address input and a data input, said binary counter being for counting memory addresses to be applied to said memory array; and

a serially loaded address buffer register having an output coupled to said binary counter data input, said address buffer register being for supplying an initial random access memory address which starts the count of said binary counter.

11. A memory circuit as claimed in Claim 10 wherein each of said first and second address generators additionally comprises:

an address offset register having an output, said address offset register storing address offset data; and

an adder having a first input coupled to said address buffer register output, a second input coupled to said address offset register output, and an output coupled to a data input of said address buffer register, said adder providing a sum of a past random access address and said address offset data to said address buffer register.

12. A memory circuit as claimed in Claim 10 wherein each of said first and second address generators additionally comprises an alternate buffer register having an output coupled to said binary counter data input, said alternate address buffer register supplying an alternate initial random access memory address which is counted by said binary counter.

13. A method of storing and providing streams of data using a random access memory array, said method comprising the steps of:

buffering the streams of data into and out from the memory array so that the stored and provided data streams occur asynchronously with operation of the memory array;

generating a random access address; and

generating a sequence of addresses initialized with said random access address said addresses being successively applied to the random access memory array.

14. A method as claimed in Claim 13 wherein said generating a random access address step comprises one step of serially loading a register with the random access address.

15. A method as claimed in Claim 13 wherein said generating a sequence step comprises the step of counting successive data items within the streams of data to generate addresses for successive application to the random access memory array.

16. A method as claimed in Claim 13 wherein said generating a sequence step generates addresses for writing the stored data stream into the array, and said method additionally comprises the step of:

generating a second sequence of addresses which are successively applied to the random access memory array for reading the provided data stream from the memory array; and

supplying, to said generating a second sequence step, a random access address which initiates the successively applied sequence of addresses.

17. A method as claimed in Claim 13 additionally comprising the steps of:

providing an address offset value; and

adding the address offset value to the random access address to generate a second random access address.

18. A method as claimed in Claim 13 additionally comprising the step of supplying, to said generating a sequence step, a second random access address which initiates a second successively applied sequence of addresses.

19. A method as claimed in Claim 13 wherein said generating a sequence step comprises the steps of:

providing an increment step value; and

adding the increment step value to a current address from the sequence of addresses to produce a next address in the sequence of addresses.